



1

Sam 2752
10/B
mm
PATENT 1-21-99

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231.

December 11, 1998
Date

Edward W. Bulchis
Edward W. Bulchis

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Brent Keeth
Application No. : 08/798,227
Filed : February 11, 1997
For : MEMORY SYSTEM WITH
DYNAMIC TIMING CORRECTION

Received

1 / 1998

Group 2700

Examiner : David Ransom
Art Unit : 2752
Docket No. : 660073.587
Date : December 11, 1998

Assistant Commissioner for Patents
Washington, DC 20231

Received

DEC 10 1998

Group 2700

AMENDMENT

Sir:

In response to the Office Action dated September 11, 1998, and the telephone interview with the Examiner conducted on Friday, December 11, please amend the application as follows:

In the Claims:

Please add new claims 20-24 as follows:

20. A method of adjusting data timing in a memory system having a memory device and a memory controller, the method comprising the steps of establishing an initial output timing at the memory device;

23

12/16/1998 SSANDARA 00000124 08/798227
01 FC:102
02 FC:103
DP
700
700
DP

B